AMENDMENTS TO THE DRAWINGS

Attached are 7 sheets of replacement formal drawings as required by the Examiner to replace the informal drawings.

REMARKS

Reconsideration and allowance are respectfully requested.

The Examiner requires formal drawings. Seven replacement sheets of formal drawings are submitted. Withdrawal of the objection to the drawings is requested.

Claims 1-8, 10-15, 17-20, 22, 24,-31, and 33-36 stand rejected under 35 U.S.C. 102(e) for anticipation by US patent publication 2003/0135699 A1 to Matsuzaki. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Matsuzaki fails to satisfy this rigorous standard.

The application describes a processor core (e.g., 10 in Figure 1)that is divided into portions including a data processing portion (e.g., 12 in Figure 1) and a memory access portion (e.g., 30 in Figure 1). The portions are independently (e.g., HCLKEN(1) and (2) in Figure 1) enabled to allow data to be transferred via the memory access interface when the processor core is sleeping.

Matsuzaki relates to a semiconductor memory device rather than to a data processor core. Multiple claim features are not disclosed in Matsuzaki. First, Matsuzaki fails to disclose "a data processor core" as recited all independent claims. The Examiner does not identify a particular element in Matsuzaki or any section of text in Matsuzaki where a processor core is disclosed. A DRAM core is a memory and not a data processor core.

Second, Matsuzaki does not disclose "a data processing portion operable to perform further data processing operations." The Examiner relies on section 0141 lines 1-4 and Figure 121 as teaching operations being performed. But these operations are not data processing operations performed by a data processing portion. Rather, those operations are performed by a memory core, which in this particular example, relate to inputting and outputting data via input/output ports.

Third, there is no memory access enable signal in Matsuzaki. The Examiner's reference to section 0553 relates to an enable signal /ENB for a read/write port PORT-B which is not a memory access enable signal.

Fourth, Matsuzaki fails to teach a data processing portion operable to receive a processor clock signal when a data processing enable signal has a predetermined value and not to receive it when it has a different value. The Examiner contends that Figure 1 "demonstrates" this limitation. Applicants disagree. Figure 1 merely shows the timing of demands received at ports A and B which are the external ports of a semiconductor memory device. The Figure shows how the read and write commands are completed within clock cycles. There is no disclosure of a data processing portion or a data processing enable signal, let alone the reception by the data processing portion of clock signals only when the enable signal has a certain value.

The fact that so many claim features are missing from Matsuzaki is not surprising because Matsuzaki relates to a different technical field and is not concerned with the same problem as are the claims in this case relating to transferring data via the processor core from a slower memory (e.g., FLASH memory) to a faster memory (e.g., instruction memory).

The application is in condition for allowance. An early notice to that effect is respectfully requested.

Respectfully submitted,

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